WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a semiconductor substrate;

a first semiconductor region of a first conduction type formed on said semiconductor substrate;

a second semiconductor region of a second conduction type opposite to said first conduction type, formed on said first semiconductor region;

a trench capacitor having a trench, said trench extending through said first semiconductor region and said second semiconductor region, said trench capacitor being formed such that its top does not reach a top surface of said second semiconductor region, said trench being formed therein with a conductive trench fill;

a pair of gate electrodes each formed on said second semiconductor region, each of said gate electrodes being positioned overlying said trench capacitor;

a pair of insulating layers each formed to cover each of said pair of gate electrodes;

a conductive layer formed between said pair of insulating layers to self-align to each of said pair of insulating layers, said conductive layer having a leading end insulated from said second semiconductor region and reaching the interior of said second semiconductor region, said conductive layer being

electrically connected to said conductive trench fill of said trench capacitor; and

a pair of third semiconductor regions of said first conduction type formed in said second semiconductor region, and positioned opposite to each other with respect to said conductive layer, each of said third semiconductor regions being directly in contact with said conductive layer, each of said pair of third semiconductor regions constituting either a source or a drain of transistors having one of said pair of gate electrodes, respectively, said pair of third semiconductor regions being formed substantially to a uniform depth.

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2. A semiconductor memory device comprising:

a semiconductor substrate;

a plurality of trench capacitors formed in said semiconductor substrate and arranged at a regular pitch;

a semiconductor layer formed on said semiconductor substrate in which said trench capacitors are formed;

an element isolation insulating film buried in said semiconductor layer to define a plurality of active element areas each spreading over two adjacent trench capacitors;

a plurality of transistors formed two by two in each of said active element areas, such that two transistors share one of source/drain diffusion layers,

and the other of said source/drain diffusion layers is positioned over regions of two adjacent trench capacitors, said transistors each having a gate connected to a word line continuous in one direction;

a contact layer for connecting the other of said source/drain diffusion layers of each of said transistors to a capacitor node layer of corresponding one of said trench capacitors; and

a bit line provided to intersect said word lines and connected to one of said source/drain diffusion layers of said transistor.

3. The semiconductor memory device according to claim 2, wherein said trench capacitors are each shaped substantially in a square having one side equal to 2F, where F is a minimum processing dimension, the diagonals of said squares are oriented in two orthogonal directions of said word line and said bit line, and said trench capacitors are arranged at a regular pitch of 1F or less in directions of two orthogonal sides of said squares.

4. The semiconductor memory device according to claim 2, wherein said trench capacitors are each shaped substantially in a square having one side equal to 2F, where F is a minimum processing dimension, the sides of said squares are oriented in two orthogonal directions of said word line and said bit line, and said trench capacitors are arranged at a regular pitch of 2F in

the bit line direction, and shifted sequentially at a one-half pitch on adjacent bit lines.

5. The semiconductor memory device according to claim 3, wherein said active element areas are arranged at a regular pitch in said bit line direction and shifted sequentially by a one-quarter pitch on adjacent bit lines.

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6. The semiconductor memory device according to claim 2, wherein said contact layer is buried such that said contact layer extends through the other of said source/drain diffusion layers to reach said capacitor node layer after said transistors have been formed.

7. The semiconductor memory device according to claim 2, wherein:

said semiconductor layer comprises a first epitaxially grown layer and a second epitaxially grown layer formed on said first epitaxially grown layer;

said contact layer is formed such that said contact layer is buried in said first epitaxially grown layer to reach said capacitor node layer before said second epitaxially grown layer is formed; and

said source/drain diffusion layers are formed after said second epitaxially grown layer has been formed, and the other of said source/drain diffusion layers has a bottom surface connected to a top surface of said contact layer.

8. The semiconductor memory device according to

claim 2, wherein said contact layer is formed such that said contact layer is buried in said semiconductor layer to reach said capacitor node layer before said transistors have been formed, and the other of said source/drain diffusion layers is connected to said contact layer through a buried diffusion layer formed in an upper side portion of said contact layer.

9. The semiconductor memory device according to claim 2, wherein said contact layer is formed such that said contact layer is buried in said semiconductor layer to reach said capacitor node before said transistors have been formed, and the other of said source/drain diffusion layers is connected to a top surface of said contact layer through a connection conductor formed on a surface thereof.

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10. The semiconductor memory device according to claim 2, wherein:

said semiconductor layer comprises a bulk semiconductor layer of another semiconductor substrate bonded to said semiconductor substrate in which said capacitors are formed, and an epitaxially grown layer formed on said bulk semiconductor layer;

said contact layer is formed such that said contact layer is buried in said bulk semiconductor layer to reach said capacitor node layer before said epitaxially grown layer is formed; and

said source/drain diffusion layers are formed

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after said epitaxially grown layer has been formed, and the other of said source/drain diffusion layers has a bottom surface connected to a top surface of said contact layer.

~~11. The semiconductor memory device according to claim 10, wherein:~~

~~a substrate isolation insulating film is interposed on a bonding surface of said semiconductor substrate and said other semiconductor substrate bonded thereto;~~

~~said element isolation insulating film includes a first element isolation insulating film buried in element isolation regions in the bit line direction to a depth at which said first element isolation insulating film reaches said substrate isolation insulating film; and a second element isolation insulating film partially overlapping said first element isolation insulating film and buried in element isolation regions in the bit line direction and word line direction to a depth shallower than said first element isolation insulating film.~~

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12. A semiconductor device comprising:

a semiconductor substrate;

an element isolation insulating film including a first insulating film buried to define active element areas on said semiconductor substrate, and a second insulating film shallower than said first insulating

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film; and

elements formed in said active element areas defined by said element isolation insulating film.

13. A method of manufacturing a semiconductor memory device comprising the steps of:

forming a plurality of trench capacitors arranged at a regular pitch on a semiconductor substrate with a capacitor node layer being covered with a cap insulating film, said cap insulating film having a surface positioned below a surface of said semiconductor substrate;

epitaxially growing a semiconductor layer on said semiconductor substrate on which said trench capacitors have been formed;

forming an element isolation insulating film on said semiconductor layer to define a plurality of active element areas such that each active element area spreads over two adjacent trench capacitors;

forming two transistors in each of said active element areas such that two transistors share one of source/drain diffusion layers, the other of said source/drain diffusion layers is positioned over regions of two adjacent trench capacitors, and gate electrodes serve as word lines continuous in one direction;

burying a contact layer between said gate electrodes, extending through the other of said

source/drain diffusion layers to reach said capacitor node layer; and

forming bit lines connected to one of said source/drain diffusion layers to intersect said word lines.

14. A method of manufacturing a semiconductor memory device comprising the steps of:

forming a plurality of trench capacitors arranged at a regular pitch on a semiconductor substrate with a capacitor node layer being covered with a cap insulating film, said cap insulating film having a surface positioned below a surface of said semiconductor substrate;

epitaxially growing a first semiconductor layer on said semiconductor substrate on which said trench capacitors have been formed;

burying a contact layer in said first semiconductor layer to reach said capacitor node layer;

epitaxially growing a second semiconductor layer on said first semiconductor layer in which said contact layer is buried;

forming an element isolation insulating film on said second semiconductor layer to define a plurality of active element areas such that each of said active element areas spreads over two adjacent trench capacitors;

forming two transistors in each of said active

element areas such that two transistors share one of source/drain diffusion layers, the other of said source/drain diffusion layers is connected to a top surface of said contact layer, and gate electrodes serve as word lines continuous in one direction; and

forming bit lines connected to one of said source/drain diffusion layers to intersect said word lines.

15. A method of manufacturing a semiconductor memory device comprising the steps of:

forming a plurality of trench capacitors arranged at a regular pitch on a semiconductor substrate with a capacitor node layer being covered with a cap insulating film, said cap insulating film having a surface positioned below a surface of said semiconductor substrate;

epitaxially growing a semiconductor layer on said semiconductor substrate in which said trench capacitors have been formed;

burying a contact layer in said semiconductor layer to reach a capacitor node layer of said trench capacitors, said contact layer having an upper end portion connected to an impurity diffusion layer formed in said semiconductor layer;

forming an element isolation insulating film on said semiconductor layer to define a plurality of active element areas such that each of said active

element areas spreads over two adjacent trench capacitors;

forming two transistors in each of said active element areas such that two transistors shares one of source/drain diffusion layers, the other of said source/drain diffusion layers is connected to said contact layer through said impurity diffusion layer, and gate electrodes serve as word lines continuous in one direction; and

forming bit lines connected to one of said source/drain diffusion layers to intersect said word lines.

~~16~~. A method of manufacturing a semiconductor memory device comprising the steps of:

forming a plurality of trench capacitors arranged at a regular pitch on a semiconductor substrate with a capacitor node layer being covered with a cap insulating film, said cap insulating film having a surface positioned below a surface of said semiconductor substrate;

epitaxially growing a semiconductor layer on said semiconductor substrate on which said trench capacitors have been formed;

burying a contact layer in said semiconductor layer to reach a capacitor node layer of said trench capacitors;

forming an element isolation insulating film on

said semiconductor layer to define a plurality of active element areas such that each of said active element areas spreads over two adjacent trench capacitors;

forming two transistors in each of said active element areas such that two transistors shares one of source/drain diffusion layers, the other of said source/drain diffusion layers is positioned on said trench capacitor region, and gate electrodes serve as word lines continuous in one direction;

forming a surface connection conductor for connecting the other of said source/drain diffusion layers to said contact layer corresponding thereto, said surface connection conductor being self-aligned to said word lines; and

forming a bit line connected to one of said source/drain diffusion layers to intersect said word line.

17. A method of manufacturing a semiconductor memory device comprising the steps of:

forming a plurality of trench capacitors arranged at a regular pitch on a semiconductor substrate with a capacitor node layer being covered with a cap insulating film;

forming a first semiconductor layer by bonding another semiconductor substrate through a substrate isolation insulating film to said semiconductor

substrate in which said trench capacitors are formed;

burying a contact layer in said first semiconductor layer to reach said capacitor node layer;

epitaxially growing a second semiconductor layer on said first semiconductor layer in which said contact layer is buried;

forming an element isolation insulating film on said first and second semiconductor layers to define a plurality of active element areas such that each of said active element areas spreads over two adjacent trench capacitors;

forming two transistors in each of said active element areas such that two transistors share one of source/drain diffusion layers, the other of said source/drain diffusion layers is connected to a top surface of said contact layer, and gate electrodes serve as word lines continuous in one direction; and

forming a bit line connected to one of said source/drain diffusion layers to intersect said word line.

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